REMARKS

This is a full and timely response to the outstanding Final Office Action mailed March 4, 2003.

I. Present Status of Patent Application

Upon entry of this response claims 1-2, 6-7, and 10-12 are pending in the present application. Claims 3, 4, and 9 have been cancelled without prejudice, waiver, or disclaimer. Applicants reserve the right to pursue the subject matter of any cancelled claims in continuation applications. Claims 11 and 12 have been added. Claims 1 and 10 have been amended as set forth above. Support for these amendments is found in the specification and in the original claims. No new matter has been added.

II. Amendments to the Specification

The specification has been amended to correct typographical errors and to provide a correct and accurate description of the invention as originally disclosed in the application. Although these amendments affect several changes to the specification, it is respectfully asserted that no new matter has been added.

III. Claims 1, 6, and 10 Comply With 35 U.S.C. §112, First Paragraph

Claims 1, 3, 6, 9, and 10 have been rejected under 35 U.S.C. § 112, first paragraph, as allegedly "containing subject matter which was not described in the specification in such a way as to reasonable convey to one skilled in the relevant art that the inventor(s) at the time the application was filed had possession of the claimed invention." The Applicants submit that claims 1, 6, and 10 define the invention in such a way as to reasonably convey to one

skilled in the relevant art that the inventors at the time the application was filed had possession of the claimed invention in the manner required by 35 U.S.C. § 112.

To show possession of the claimed invention, the Applicant must describe the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, (Fed. Cir. 1997). There is a strong presumption that an adequate written description of the claimed invention is present when the application is filed. *In re Wertheim*, 541 F2.2d 257. 263 (CCPA 1976).

A. The Office Action Lacks a *Prima Facie* Showing of a Lack of Possession

A description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the Examiner to rebut the presumption. See *In re Marz*occhi, 439 F.2d 220, 224 (CCPA 1971). The Examiner has the initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize in an Applicant's disclosure a description defined by the claims. *Wertheim*, 541 F.2d at 263.

In fact, a two-prong checklist for a rejection under 35 U.S.C. §112, second paragraph is outlined in MPEP 2163 §III.A. The first prong requires that the findings "[i]dentify the claim limitation at issue." The second prong requires that the findings "[e]stablish a *prima facie* case by **providing reasons why a person skilled in the art at the time the application was filed would not have recognized that the inventor was in possession of the invention as claimed in view of the disclosure of the application as filed.**" *Emphasis added*, MPEP 2163 §III.A.

The sum total of the reason alleged in the Office Action for rejecting claims 1, 3, 6, 9, and 10 under 35 U.S.C. §112, second paragraph is:

> Discussion of the parasitic capacitance and parasitic effects are seen throughout pages 7-13 of the specification. However, none of the discussion demonstrates the reduction in parasitic capacitance or as to how the parasitic capacitance or the parasitic effects being reduced as recited in claims 1, 3, 6, 9 and 10.

(Office Action, pg. 2). Applicants submit that this brief statement falls far short of the legal requirement for establishing a *prima facie* case of a lack of possession of the invention. The Office Action fails to state with any particularity as to why someone skilled in the art at the time the application was filed would not have recognized that the inventor was in possession of the invention as claimed in view of the disclosure of the application as filed. Rather, the allegation is a mere conclusory allegation that "none of the discussion demonstrates the reduction in parasitic capacitance or as to how the parasitic capacitance or the parasitic effects being reduced as recited in claims." This is an improper attempt to shift the legal burden to the Applicants.

Thus, Applicants submit that the Office Action has not made a prima facie showing of the Applicants' lack of possession of the invention, and requests that the rejection to claims 1, 6, and 10 under 35 U.S.C. §112, first paragraph, be withdrawn.

B. Applicants Have Defined the Invention in Such a Way as to Reasonably Convey to One Skilled in the Relevant Art that the Inventor(s), at the Time the Application was Filed, Had Possession of the Claimed Invention

Even assuming, *arguendo*, that the rejection of claims 1, 3, 6, 9, and 10 is proper, the Applicants have defined the invention in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention in the manner required by 35 U.S.C. § 112.

First, as an initial clarification, it is known that the parasitic characteristics of a transistor device are predetermined and fixed at the time of manufacture. These

predetermined characteristics are acknowledged and described in the detailed description (pg. 5, line 20 – pg. 7, line 8), as well as in FIG. 3 and FIG. 4.

Specifically, FIG. 4 shows the relevant parasitic capacitance and resistance of a transistor device when a bias voltage is applied to the control signal. The parasitic resistance (or "on resistance") is represented by resistor 404 which stretches across nodes 112 and 116 (pg. 6, lines 21-24). The parasitic capacitance is not one capacitance, but rather is measured across three node pairs. Specifically, capacitor 404 represents the parasitic capacitance between nodes 112 and 116. Capacitor 400 represents the parasitic capacitance between node 112 and 114. Finally, capacitor 402 represents the parasitic capacitance between node 114 and 116 (pg. 6, lines 23-28).

The circuitry, as in claims 1, 6, and 10, is not configured to actually change the predetermined parasitic capacitance or resistance of a transistor device, but rather to reduce the "parasitic effects" of a transistor device in an overall circuit (pg. 8, line 10). These "parasitic effects" may also be referred to in the disclosure as the "overall parasitic resistance" or "overall parasitic capacitance" of the device (pg. 1, lines 26-27 or see pg. 8, lines 28-30). While a device has an inherent parasitic capacitance and resistance, the "effect" of this capacitance or resistance can be minimized by configuring the transistor with various circuit components in the manner suggested in the detailed description. The resulting "effect" of the circuit configuration results in a lowered parasitic "effect" at particular nodes of the circuit.

It is first helpful to demonstrate the circuit configuration and associated parasitic capacitance and resistances of a transistor device without using the configurations as suggested in the application. FIG. 5 represents an AC simplified diagram of a transistor circuit when a voltage bias is applied to enable the switch 118 of a transistor. Note that the

parasitic capacitance 402 is removed because node 118, as known in the art, is electrically an AC ground (pg. 7, lines 9-11).

FIG. 6 represents an AC simplified diagram of a transistor when no voltage bias is applied to the switch 118. Note that parasitic resistance 404 is not present since there is no electrical connectivity, and thus no current, between nodes 112 and 116 when the switch is disabled. Note also that the only parasitic capacitance present is represented by capacitors 400 and 404 (pg. 6 lines 13-15).

Independent Claim 1

Specifically, as to claim 1, the Office Action alleges that the specification fails to describe how "**the impedance circuit configured with a sufficiently high impedance to reduce the parasitic capacitance between the first terminal and the second terminal of the transistor by preventing the third switch node from functioning as an alternating current ground during operation of the switch.**" Further, the Office Action alleges "none of the discussion [in pages 7-13 of the specification] demonstrates the reduction in parasitic capacitance or as to how the parasitic capacitance or the parasitic effects being reduced as recited in claims 1, 3, 6, 9 and 10."

As to claim 1, it is helpful to refer to FIG. 7 – FIG. 10. FIG. 7 represents the general circuit diagram, including impedance circuit 708, without representation of any parasitic capacitance or resistance. FIG. 8 is a circuit diagram showing the circuit of FIG. 7, showing the parasitic capacitance and resistance of the transistor device when a voltage bias is applied to the switch terminal 710 (pg. 8, lines 15-17). A comparison of FIG. 7 (applying the Applicants' circuitry) to FIG. 5 (without the Applicants' circuitry) demonstrates that the parasitic capacitance 802 between node 712 and 716 has returned with the addition of impedance circuit 708.

The detailed description fully describes why the addition of impedance circuit 708, and the resulting parasitic capacitance formed between nodes 712 and 716 actually reduce the effective parasitic capacitance between nodes 714 and 716:

> As illustrated in FIG. 9, the presence of impedance element 708 in transistor circuit 700 creates an AC open at switch terminal 710 instead of an AC short as in the prior art. Therefore, capacitor 800 and 802 are connected in series, and can be simplified to a capacitor 900 having a capacitance (Cseries) defined by the following equation:
>
> $$Cseries = \frac{(C1,3)(C1,2)}{C1,3 + C1,2}$$

(amended, pg. 8, line 29 – pg. 9, line 5)

Thus, as is evident from the formula, the total capacitance of capacitors connected in series is less than the capacitance of the individual capacitors. The examiner is encouraged to compare FIG. 5 (showing an AC simplified diagram of a transistor without an impedance circuit configured like claim 1) to FIG. 8 (showing the parasitic capacitance between nodes of a transistor when an impedance circuit is attached as in claim 1). Since capacitors 800 and 802 in FIG. 9 are combined in series, the effective capacitance between nodes 714 and 716 is lower than the effective capacitance between equivalent nodes 112 and 116 in FIG. 5.

Thus, the Applicants submit that the disclosure has conveyed, with reasonable certainty, to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention of claim 1. Specifically, the disclosure does show how the impedance circuit is "configured with a sufficiently high impedance to reduce the effective parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch" as in claim 1. The Applicants request the rejection to claim 1 be withdrawn and the claim allowed. Similarly, the rejection under

§112 of claim 2 (which depends from claim 1), should also be withdrawn for at least the same reason.

Independent Claim 6 and Dependent Claim 10

Specifically, as to claim 6, the Office Action alleges that the specification fails to describe how "**the third transistor device configured with predetermined parasitic characteristics that improve the effective parasitic characteristics of the transistor circuit.**" Further, the Office Action alleges "none of the discussion [in pages 7-13 of the specification] demonstrates the reduction in parasitic capacitance or as to how the parasitic capacitance or the parasitic effects being reduced as recited in claims 1, 3, 6, 9 and 10."

As to claims 6 and 10, it is helpful to refer to FIG. 2 and FIG. 12 - FIG. 16. FIG. 2 depicts a transistor circuit for implementing a differential switch (see pg. 5, lines 20-30). FIG. 12 represents a differential circuit as in FIG. 2, however a third transistor device 1220 has been added, as in claim 6, to improve overall parasitic effects of the circuit by reducing the parasitic resistance of the circuit, with a less than equivalent increase in capacitance. FIG. 13 depicts the circuit of FIG. 12 with the parasitic capacitance and resistances illustrated when the transistor devices 1210, 1212, and 1220 are enabled as switches.

FIG. 14 simplifies FIG. 13 by illustrating the equivalent differential half-circuit diagram. Block 1410 is the simplified representation of the parasitic characteristics of transistor device 1210. Similarly, block 1410 represents the simplified representation of the parasitic characteristics of transistor device 1220 (pg. 12, lines 22-29).

FIG. 15 shows **block 1420** of FIG. 14 in a simplified circuit diagram. FIG. 16 further simplifies the **entire** diagram of FIG. 14 **where** $C_{1600}=2 * C_{1502}$ **and** $R_{1602}=R_{1504}/3$ (pg. 13, lines 1-25). One skilled in the art at the time of the invention could certainly add resistors

1304 and 1325, as well as capacitance 1300, 1302, 1316, and 1320 to arrive at the conclusion above.

For instance, assuming the transistors are manufactured similarly, each parasitic capacitance and resistance representation will be equal in value (p. 13, lines 5-8). Note that "resistor 1325 has one-half the resistance of resistor 1304 because the circuit is a differential half-circuit diagram" (pg. 12, lines 29-30). Adding parasitic capacitance 1316 and 1320 (of transistor 1410) to parasitic capacitance 1300 and 1302, doubles the effective parasitic capacitance of the entire circuit as it existed before adding the third transistor (pg. 13, lines 15-18). For example:

The total capacitance of transistor 1210 is represented in block 1420 of FIG. 14:

$$C_{1420} = C_{1300} + C_{1302} = 2C$$

The total capacitance of the entire circuit, now including the third transistor 1410, is represented by:

$$C_{1600} = C_{1300} + C_{1302} + C_{1316} + C_{1320} = 4C$$

4C is double 2C. Thus, by adding the third transistor, the effective parasitic capacitance has been doubled.

The parallel addition of parasitic resistance 1325, and 1304 decreases parasitic resistance by a factor of 3 (pg. 13, lines 19-25). For example:

$$R_{1602} = [1/R + 1/(1/2)R] = [1/R + 2/R] = [3/R] = 1/3R_{1504}$$

Thus, by adding the third transistor in the manner described in claim 3, the effective parasitic capacitance has been doubled, but the effective resistance has decreased by a factor of 3 (pg. 14, lines 4-17). Thus, the third transistor device is "**configured with predetermined parasitic characteristics that improve the effective parasitic characteristics of the transistor circuit**" as in claim 6. Further, "**the predetermined parasitic characteristics of the third transistor device reduce the effective parasitic**

resistance of the transistor circuit while sustaining a less than equivalent increase in effective parasitic capacitance of the transistor circuit" as in claim 10.

Thus, the Applicants assert that the application has conveyed, with reasonable certainty, to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention of claims 6 and 10. Applicants request that the rejection to claims 6 and 10 be withdrawn and the claims allowed. Similarly, the rejection under §112 of claim 7 (which depends from claim 6), should also be withdrawn for at least the same reason.

Claims 3, 4, and 9

Claims 3 and 9 have been cancelled, therefore the rejection as to these claims under 35 U.S.C. §112, first paragraph is believed to be moot. Furthermore, claim 4 has been cancelled, therefore the rejection as to this claim under 35 U.S.C. 112 (for the alleged technical deficiency of claim 3 is moot).

IV. Claims 1, 2, and 10 Comply With 35 U.S.C. §112, Second Paragraph

The Office Action rejects claims 1, 2, 3, 9, and 10 under 35 U.S.C. §112, second paragraph, as allegedly being "indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention."

A. Claim 1 and 2 Particularly Point Out and Distinctly Claim the Subject Matter Regarded as the Invention

Specifically, as to claim 1 (and dependent claim 2), the Office Action alleges the language claiming "the impedance circuit configured with a sufficiently high impedance **to reduce the parasitic capacitance** between the first terminal and the second terminal of the transistor device, by preventing the third switch node from function as an alternating current

ground during operation of the switch" is "indefinite because it is misdescriptive." The Office Action takes note that the parasitic capacitance of a device cannot be changed or reduced, but rather "compensated."

Applicants respectfully disagree with the assertion in the Office Action that the recitation of the language "to reduce the parasitic capacitance" in claim 1 is indefinite. Again, it is known that the parasitic characteristics of a transistor device are predetermined and fixed at the time of manufacture. The predetermined characteristics are acknowledged and described in the detailed description (pg. 5, line 20 – pg. 7, line 8), as well as in FIG. 3 and FIG. 4. Thus, the circuit configuration of claims 1 and 2 reduce the parasitic effects, rather than the inherent parasitic characteristics of the transistor device (pg. 5, line 20 – pg. 7, line 8).

However, in the interest of furthering prosecution, and to avoid any possible confusion, the language of claim 1 has been amended as indicated above, the language clearly setting forth that the impedance circuit is "configured with a sufficiently high impedance to reduce the **effective** parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch."

Thus, the circuitry of claims 1 and 2 is not configured to actually change the predetermined parasitic capacitance or resistance of a transistor device, but rather to reduce the "parasitic effects" of a transistor device "between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch" (pg. 8, line 10). These "parasitic effects" may also be referred to in the disclosure as the "overall parasitic resistance" or "overall parasitic capacitance" of the device (pg. 1, lines 26-27 or see pg. 8, lines 28-30). While a device has an inherent parasitic capacitance and resistance, the "effect"

of this capacitance or resistance can be minimized by configuring the transistor with various circuit components in the embodiments suggested in the detailed description. The resulting "effect" of the configuration results in a lowered parasitic "effect" at particular nodes of the circuit.

Applicants wish to clarify that the foregoing amendment has been made for purposes of better defining the invention in response to the rejections made under 35 U.S.C. § 112, and not in response to the rejections made based on a prior art reference. Indeed, Applicants submit that no substantive limitations have been added to the claims. Applicants further submit that this merely cosmetic amendment is non-narrowing and, pursuant to *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S. Ct. 1831 (2002), no prosecution history estoppel arises from these amendments.

Therefore, Applicants respectfully assert that the language "**effective** parasitic capacitance" in independent claim 1 is not indefinite. Rather, this language clearly points out and distinctly claims the subject matter which Applicants regard as the invention. Accordingly, Applicants request that the Examiner reconsider and withdraw the rejection of independent claim 1 (and claim 2 which depends from claim 1) under 35 U.S.C. §112, second paragraph.

B. Claim 10 Particularly Points Out and Distinctly Claims the Subject Matter Regarded as the Invention

As to claim 10, which directly depends from claim 6, the Office Action alleges the phrase "while sustaining a less than equivalent increase in resistance of the transistor circuit" is indefinite because it is unclear.

The language cited in the Office Action as indefinite in claim 10 is not found in claim 10, but rather claim 9 Because claim 9 is cancelled, the rejection is believed to be moot.

However, in that claim 10 recites similar language to claim 9, Applicants have amended claim 10 in order to preempt any possible confusion as to what the claim means by "a less than equivalent increase in capacitance of the transistor circuit." Specifically, claim 10 has been amended to clarify that the circuit configuration does not change the **inherent** parasitic capacitance of any particular transistor, but rather improves the **effective** parasitic characteristics.

Applicants wish to clarify that the foregoing amendment has been made for purposes of better defining the invention in response to the rejections made under 35 U.S.C. § 112, and not in response to the rejections made based on a prior art reference. Indeed, Applicants submit that no substantive limitations have been added to the claims. Applicants further submit that this merely cosmetic amendment is non-narrowing and, pursuant to *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S. Ct. 1831 (2002), no prosecution history estoppel arises from these amendments.

Therefore, Applicants respectfully submit that the language "while sustaining a less than equivalent increase in **effective parasitic capacitance** of the transistor circuit" in independent claim 10 is not indefinite. Rather, this language clearly points out and distinctly claims the subject matter which Applicants regard as the invention. Accordingly, Applicants request that the Examiner reconsider and withdraw the rejection of independent claim 10 under 35 U.S.C. §112, second paragraph.

C. The Rejection of Claims 3 and 9 Under §112, Second Paragraph are Moot

Claims 3 and 9 have been cancelled, therefore the rejection as to these claims under 35 U.S.C. §112, second paragraph is moot.

V. Claims 1 and 2 are Patentable Over U.S. Patent No. 4,678,947 to *Huijsing*

The Office Action rejects claims 1 and 2 under 35 U.S.C. §102(b) as being anticipated by Huijsing. Specifically, the Office Action argues that FIG. 2 of Huijsing shows all of the features of the transistor circuit of claims 1 and 2.

Applicants' claim 1 recites:

> 1. A transistor circuit for implementing a switch, comprising:
> a first switch node configured to connect to an external circuit;
> a second switch node configured to connect to the external circuit;
> a transistor device having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;
> a third switch node for receiving the control signal; and
> **an impedance circuit connected to the third switch node and the third terminal of the transistor device, the impedance circuit configured with a sufficiently high impedance to reduce the effective parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch.**

(*Emphasis added.*) Applicants respectfully submit that claim 1 is patentable over the Huijsing reference for at least the reason that the Huijsing reference fails to disclose the features emphasized above in bold text.

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of *each element* of the claim under consideration." W. L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983)(emphasis added). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102(b).

The Office Action alleges that elements "(A1, R1, R2, 14, A2)" make up an impedance circuit. Further the Office Action alleges that the circuit (A1, R1, R2, 14, A2) is "configured with a sufficiently high impedance (col 4 lines 43-44) to 'reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device' by

preventing the third switch node from functioning as an alternating current ground during operation of the switch." Specifically, the Office Action alleges "that the impedance circuit (A1, R1, R2, 14, A2) isolates the input (CT) from the third switch node (N1) thus, in an AC operation, the voltage at node (N1) is not pulled to ground and the high impedance of circuit (A1, R1, R2, 14, A2) provides a very low droop rate."

In the present case, not every feature of the claimed invention is represented in the Huijsing reference. As an initial matter, Huijsing does not disclose "an impedance circuit ... configured with a sufficiently high impedance to reduce the effective parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch."

The portion of Huijsing cited in the Office Action recites that because "CT input terminal **is a high-impedance input**, the circuit functions as a rectifier by simply interconnecting terminals CT and T1" (*emphasis added*, col. 4 lines, 43-45). However, this indicates that the impedance of Huijsing is at the **input** (CT), not the **output** (N1) of the alleged impedance device. The input impedance at CT is irrelevant. Rather, the relevant impedance is that of node N1.

The Huijsing circuit will not prevent the third switch node from acting as an AC ground because the impedance is not high at node N1. Huijsing discloses that "the amplifier input currents are then very small compared to the R1 and R2 currents" (col 5, 23-26). Further, the current supply 14 provides current of (Va + V12)/R1. Thus, circuit of (A1, R1, R2, 14, A2) does not provide the necessary high impedance looking from the switch of transistor Q0 as alleged in the Office Action. Thus, because the impedance **at node N1** is low, the circuit of Huijsing actually increases the effective parasitic capacitance between the first terminal and the second terminal of the transistor device.

Referring to FIG. 4, recall that without the necessary impedance at the switch node 118, switch node 118 becomes an electrical AC ground and therefore the capacitance between terminal 114 and terminal 116 is **removed** (pg. 8, lines 25-28). **Without capacitance 402, the effective parasitic capacitance between the first terminal and the second terminal of the transistor device is increased**. Thus, to decrease effective parasitic capacitance between the first terminal and the second terminal of the transistor device, the object is to "prevent the third switch node from functioning as an AC ground by adding a sufficiently high impedance." As shown in FIG. 8, the addition of sufficiently high impedance at node 712 (looking back towards node 710), creates an AC open at switch terminal 710 instead of a short as in FIG. 4. Therefore, capacitor 800, and 802 are connected in series. As one skilled in the art knows, the effective capacitance of capacitors connected in series is less than the capacitance of the individual capacitors. Thus, the effective parasitic capacitance is decreased between the first terminal and the second terminal of the transistor device.

Accordingly, and for at least the reasons set forth above, independent claim 1 is believed to be allowable over the Huijsing. Furthermore, because claim 1 is believed to be allowable, dependent claim 2 (which depends on independent claim 1) should be allowable as a matter of law for at least the reason that claim 2 contains all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Applicants request that the Examiner reconsider and withdraw the rejection of claims 1 and 2 under 35 U.S.C. §102(b).

VI. The Rejection of Claims 3 and 4 Under 35 U.S.C. § 102(b) are Moot

Claims 3 and 4 have been rejected under 35 U.S.C. 102(b) as alleged in the Office Action. Applicants submit that claims 3 and 4 are patentable over Chiba. However, in view of the cancellation of claims 3 and 4, the 102(b) rejection of the foregoing claims is rendered moot.

VII. Claims 6, 7, and 10 are Patentable Over U.S. Patent No. 5,559,451 to *Okamura*

The Office Action rejects claims 6, 7, 9, and 10 under 35 U.S.C. §102(b) as being anticipated by Okamura.

Claims 6 and 7

The Office Action alleges that FIG. 5 of Okamura discloses the transistor circuits of claims 6 – 7.

Applicants' claim 6 recites:

> 6. A transistor circuit **for implementing a differential switch,** comprising:
>
> a first switch node configured to connect to an external circuit;
>
> a second switch node configured to connect to the external circuit;
>
> a first transistor device having a first terminal connected to the first switch node, a second terminal, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;
>
> a second transistor device having a first terminal connected to the second terminal of the first transistor device, a second terminal connected to the second switch node, and a third terminal configured to receive the control signal; and
>
> a third transistor device having a first terminal connected to the first terminal of the first transistor device, a second terminal connected to the second terminal of the second transistor device, and a third terminal configured to receive the control signal, **the third transistor device configured with predetermined parasitic characteristics that improve the effective parasitic characteristics of the transistor circuit.**

(*Emphasis added.*) Applicants respectfully submit that claim 1 is patentable over Okamura for at least the reason that Okamura fails to disclose the features emphasized above in bold text.

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of *each element* of the claim under consideration." W. L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983)(emphasis added). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102(b).

Here, Okamura does not disclose a "transistor circuit for implementing **a differential switch**" or that **"the third transistor device configured with predetermined parasitic characteristics that improve the effective parasitic characteristics of the transistor circuit"** as required in claim 6.

First, the circuitry of transistors 21, 22, and 23 does not comprise a "transistor circuit **for implementing a differential switch**," but rather is configured in a single ended manner using ground as the reference voltage. Implementing the switch in a differential configuration is integral to the way the circuit performs. When the circuit is configured as a differential switch, the node between the first and second transistor acts as a virtual ground, thus causing the value of the parasitic resistance across the third transistor to be one-half the value of the parasitic resistance of the first transistor (pg. 12 lines 29-30). Because of the inverse relationship of capacitance and resistance, it is the halved parasitic resistance across the third transistor that mathematically results in a reduction of the effective resistance while sustaining a less than equivalent increase in effective capacitance of the transistor circuit when configured as in claim 9.

Second, Okamura does not disclose a third transistor device "**configured with predetermined parasitic characteristics that improve the effective parasitic**

characteristics of the transistor circuit." The Office Action alleges that Okamura discloses that "when the third transistor 23 is turned on, its parasitic capacitances is [sic] connected in parallel with the parasitic capacitances of the first and second transistors thus, the parasitic characteristics of the transistor circuit is changed accordingly (improved)." However, transistor 21 is a p-channel transistor and transistor 22 and 23 are n-channel transistors (Okamura, FIG. 5). Thus, when a signal is applied to IN, transistor 21 is disabled and transistors 22 and 23 are enabled (col. 5, lines16-19 and 46-48). Further, when 22 and 23 are enabled, transistor 42 is disabled (col. 36-38, FIG. 6D, FIG. 6A). Because transistor 42 is not enabled there is no current through transistor 23. Thus, transistor 23 does not carry a parasitic resistance. Thus, even if the capacitance of transistor 22 and 23 are put into parallel as alleged, this would only **increase** the parasitic capacitance **without decreasing** the effective parasitic resistance.

Accordingly, and for at least the reasons set forth above, independent claim 6 is believed to be allowable over Okamura. Furthermore, because independent claim 6 is believed to be allowable over the prior art of record, dependent claims 7 and 10 (which depend from independent claim 6) are allowable as a matter of law for at least the reason that they contain all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, the Examiner is respectfully requested to withdraw this rejection and place claims 6, 7, and 10 in condition for allowance.

Claim 9

Claim 9 has been rejected under 35 U.S.C. 102(b) as alleged in the Office Action. Applicants submit that claims 9 is patentable over Okamura. However, in view of the cancellation of claims 9, the 102(b) rejection of the foregoing claim is rendered moot.

Claim 10

The Office Action alleges "because of the effect of the parallel connection of the transistors of the circuit, the equivalent resistance of the circuit is less than the resistance of the transistors and the capacitance is increased."

As an initial matter, the circuitry of transistors 21, 22, and 23 does not comprise a "transistor circuit **for implementing a differential switch**," but rather is configured in a single ended manner using ground as the reference voltage. Implementing the switch in a differential configuration is integral to the way the circuit performs. When the circuit is configured as a differential switch, the node between the first and second transistor acts as a virtual ground, thus causing the value of the parasitic resistance across the third transistor to be one-half the value of the parasitic resistance of the first transistor (pg. 12 lines 29-30). Because of the inverse relationship of capacitance and resistance, it is the halved parasitic resistance across the third transistor that mathematically results in a reduction of the effective resistance while sustaining a less than equivalent increase in effective capacitance of the transistor circuit when configured as in claim 9.

Second, the Office Action does not even allege Okamura shows the claimed feature that "the predetermined parasitic characteristics of the third transistor device reduce the effective parasitic resistance of the transistor circuit while sustaining **a less than equivalent** increase in effective parasitic capacitance of the transistor circuit." Instead, the Office Action alleges that the increase in capacitance is **equivalent** to the decrease in resistance. This shows a fundamental misunderstanding of what the Applicants have claimed.

Third, Okamura does not contain the limitation of "the predetermined parasitic characteristics of the third transistor device reduce the effective parasitic resistance of the transistor circuit **while sustaining a less than equivalent increase in effective parasitic capacitance of the transistor circuit**" as in claim 10. For example, transistor 21 is a p-

channel transistor and transistor 22 and 23 are n-channel transistors (FIG. 5). Thus, when a signal is applied to IN, transistor 21 is disabled and transistors 22 and 23 are enabled (col. 5, lines16-19 and 46-48). Further, when 22 and 23 are enabled, transistor 42 is disabled (col. 36-38, FIG. 6D, FIG. 6A). Because transistor 42 is not enabled there is no current through transistor 23. Thus, transistor 23 does not carry a parasitic resistance. In conclusion, even if the capacitance of transistors 22 and 23 are put into parallel as alleged, this would only **increase** the parasitic capacitance **without decreasing** the effective parasitic resistance **at all.**

Accordingly, and for at least the reasons set forth above, independent claim 10 is believed to be allowable over Okamura. Accordingly, the Examiner is respectfully requested to withdraw this rejection and place claim 10 in condition for allowance.

VIII. Claim 2 is Patentable Over U.S. Patent No. 4,678,947 to *Huijsing*

The Office Action rejects claim 2 under 35 U.S.C. §103(a) as being anticipated by Huijsing. Specifically, the Office Action alleges that Huijsing discloses the Applicants' invention substantially as claimed with the exception of "the transistor device is [sic] MOSFET transistor." The rejection concludes, however, that it would have been obvious to a person having ordinary skill in the art "to replace bipolar transistor Q0 of Huijsing with a MOSFET transistor."

As identified above in reference to independent claim 1 (from which claim 2 directly depends), Huijsing does not teach, disclose, or suggest an impedance circuit **"configured with a sufficiently high impedance to reduce the effective parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch"** as in application claims 1 and 2. In that the knowledge of one skilled in the art does not remedy this deficiency of the Huijsing reference, the Applicants respectfully submit

that claim 2, which depends from claim 1, are allowable Huijsing for the same reason that independent claim 1 is allowable over Huijsing. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Applicants request that the Examiner reconsider and withdraw the rejection of claim 2 under 35 U.S.C. §103(a).

CONCLUSION

In light of the foregoing remarks and for at least the reasons set forth above, Applicants respectfully submit that all rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-2, 6-7, 10-12 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Washington D.C. 20231, on 5/2/03.

Stephanie Riley
Signature